

BLF188XR; BLF188XRS

Power LDMOS transistor

Rev. 5 — 12 November 2013

Product data sheet

1. Product profile

1.1 General description

A 1400 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 600 MHz band.

Table 1. Application information

Test signal	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)
CW	2 to 30	50	1270	29.0	75
	27	50	1400	23.7	73
	41	50	1200	22.0	82
	60	48	1240	22.0	77
	72.5	50	1350	23.1	83
	81.4	50	1200	27.1	77.8
	88 to 108	50	1320	22.5	85
	108	50	1200	26.5	83
	200	50	1288	19.3	68.3
pulsed RF	81.4	50	1200	25.8	85
	81.4	50	1400	25.4	81
	108	50	1400	24.0	73
DVB-T	174 to 230	50	225	23.8	29

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

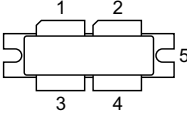
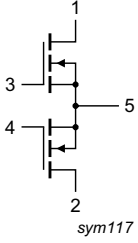
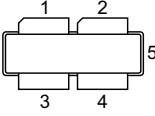
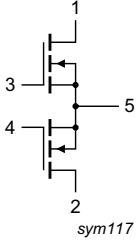
1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF188XR (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		
BLF188XRS (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF188XR	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF188XRS	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	135	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[1]	225	°C

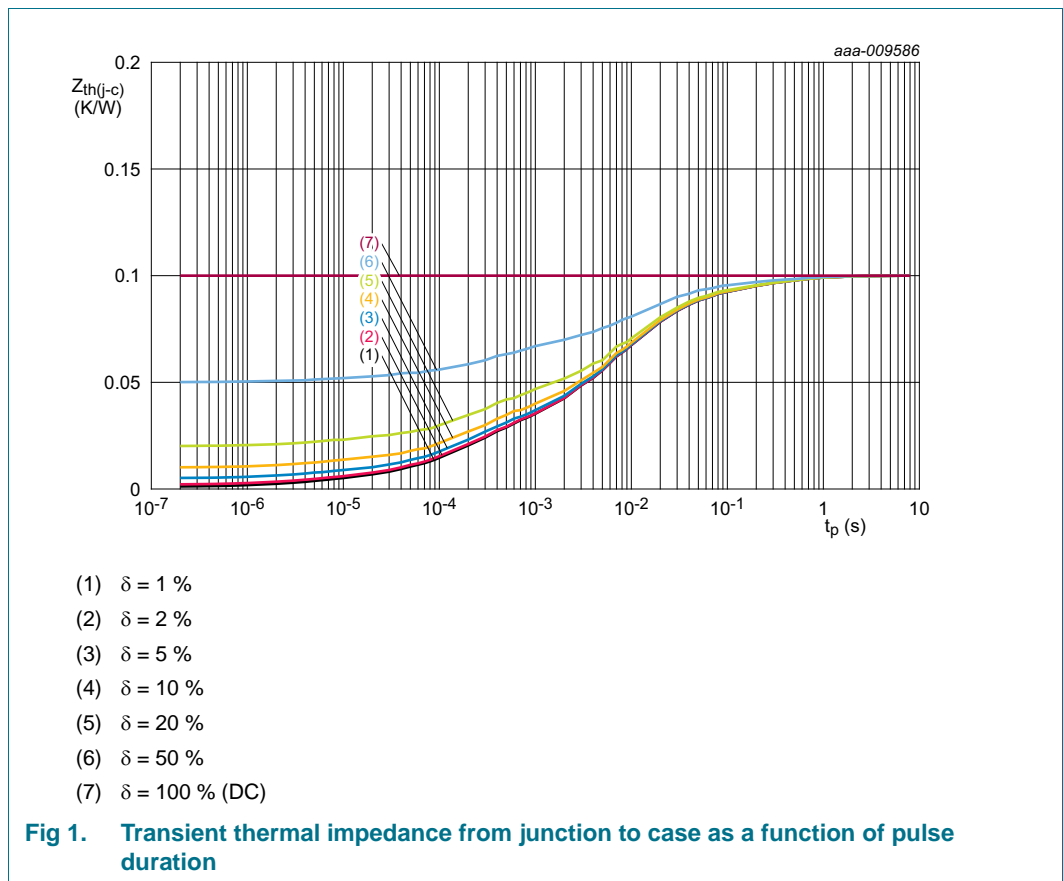
[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 150\text{ }^\circ\text{C}$	[1][2] 0.10	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_j = 150\text{ }^\circ\text{C}; t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	[3] 0.03	K/W

- [1] T_j is the junction temperature.
- [2] $R_{th(j-c)}$ is measured under RF conditions.
- [3] See [Figure 1](#).



6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 5.5\text{ mA}$	135	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 550\text{ mA}$	1.25	1.9	2.25	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50\text{ V}; I_D = 20\text{ mA}$	0.68	1.5	1.88	V

Table 6. DC characteristics ...continued
 $T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

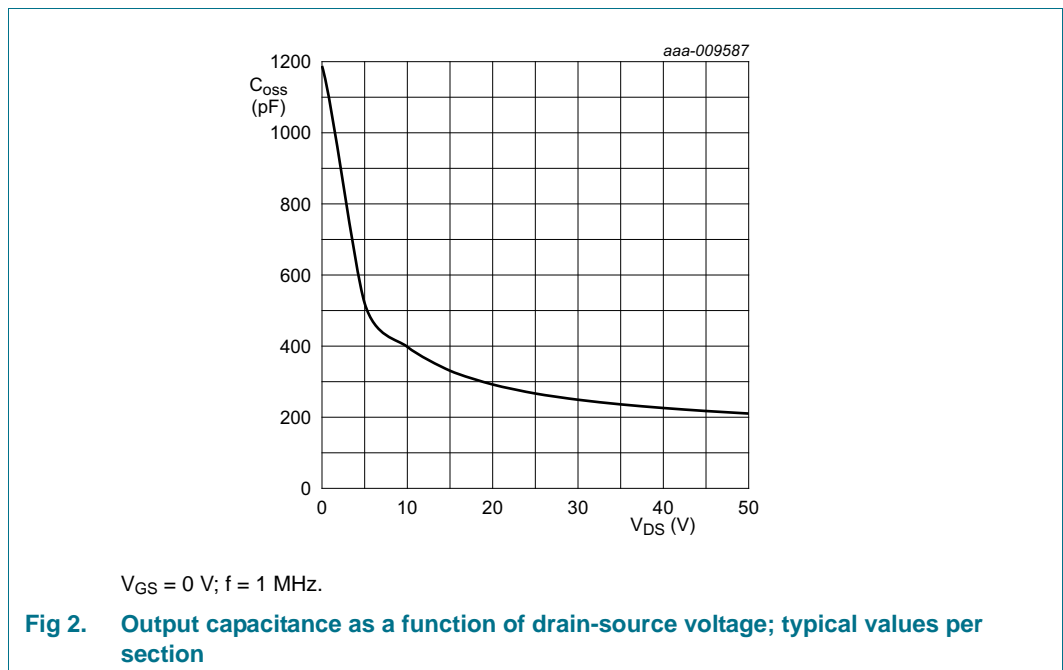
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	77	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 19.25\text{ A}$	-	0.08	-	Ω

Table 7. AC characteristics
 $T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	6.2	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	582	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	212	-	pF

Table 8. RF characteristics
 Test signal: pulsed RF; $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\%$; $f = 108\text{ MHz}$; RF performance at $V_{DS} = 50\text{ V}$; $I_{Dq} = 40\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 1400\text{ W}$	23.2	24.4	-	dB
RL_{in}	input return loss	$P_L = 1400\text{ W}$	-	-21	-14	dB
η_D	drain efficiency	$P_L = 1400\text{ W}$	69	73	-	%



7. Test information

7.1 Ruggedness in class-AB operation

The BLF188XR and BLF188XRS are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{DQ} = 40\text{ mA}$; $P_L = 1400\text{ W}$ pulsed; $f = 108\text{ MHz}$.

7.2 Impedance information

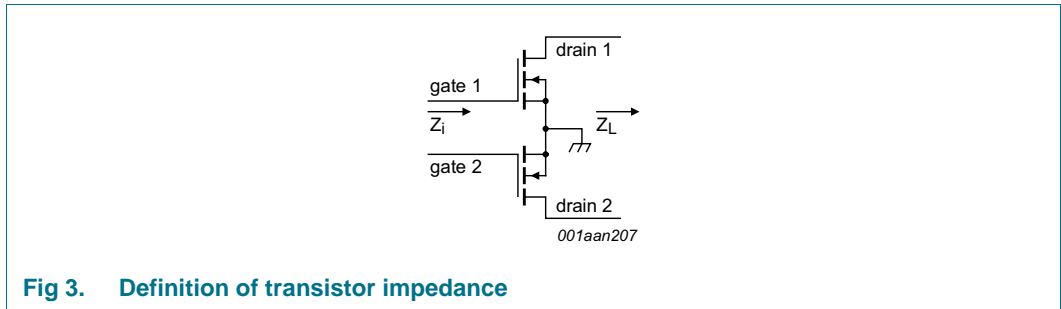


Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at $V_{DS} = 50\text{ V}$ and $P_L = 1400\text{ W}$.

f (MHz)	Z_i (Ω)	Z_L (Ω)
108	$2.94 - j9.64$	$2.74 + j0.57$

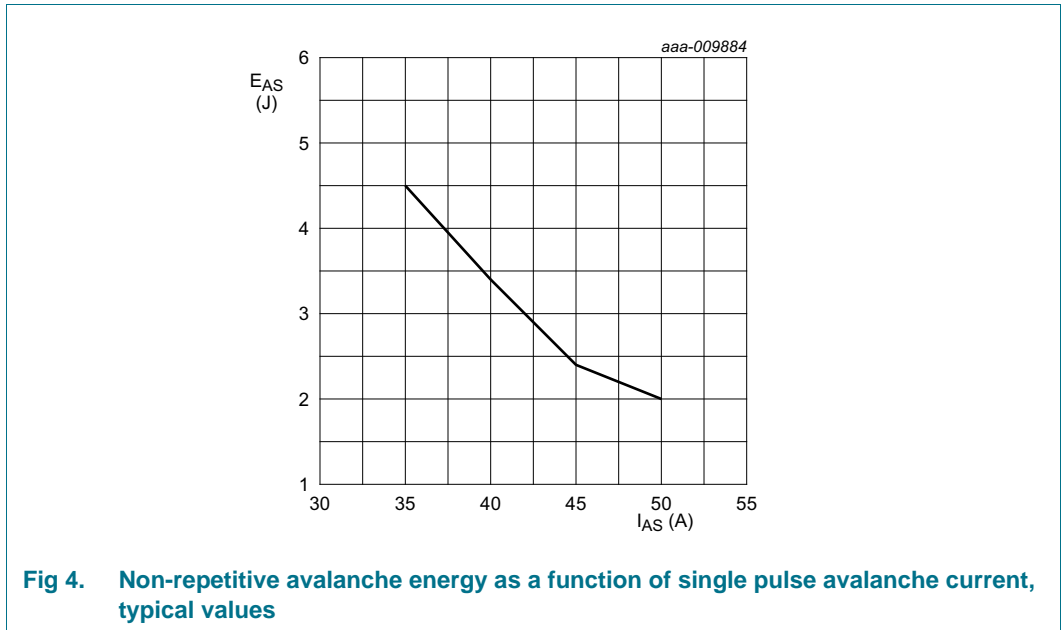
7.3 UIS avalanche energy

Table 10. Typical avalanche data per section

$T_{amb} = 25\text{ }^\circ\text{C}$; typical test data; test jig without water cooling.

I_{AS} (A)	E_{AS} (J)
35	4.5
40	3.4
45	2.4
50	2.0

For information see application note "AN10273".



7.4 Test circuit

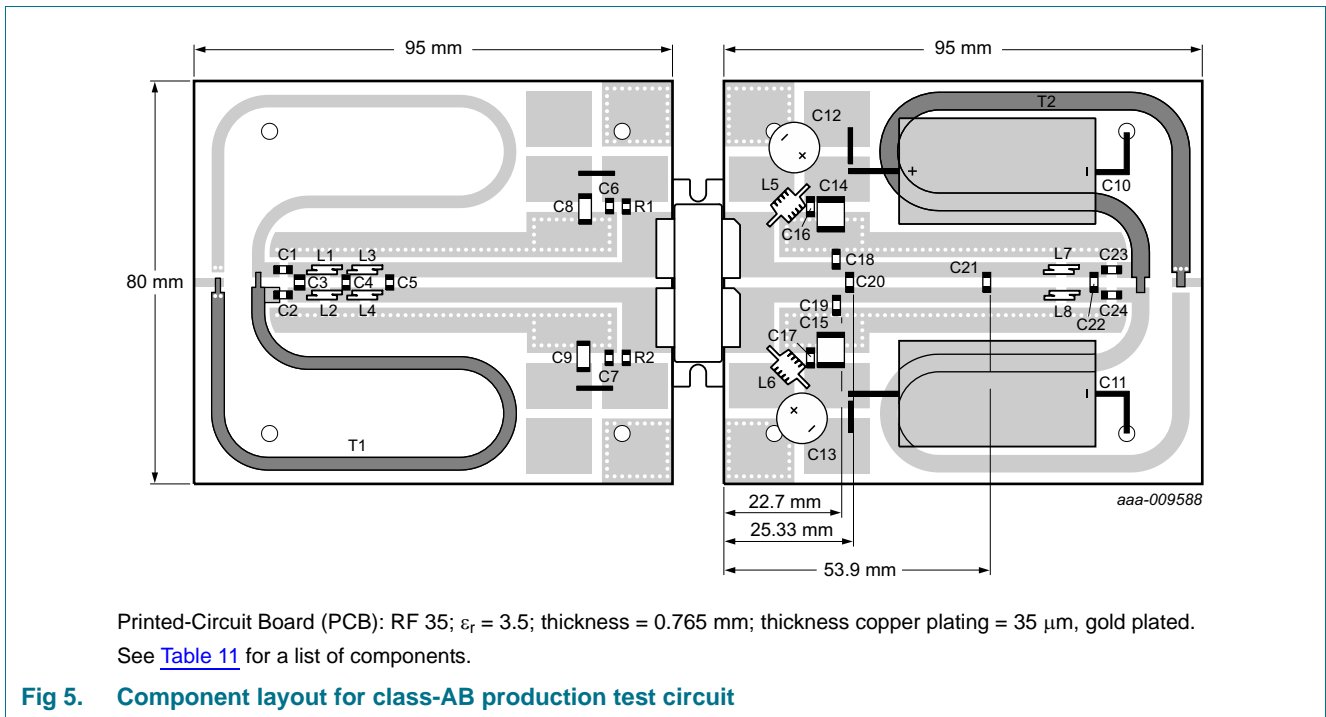


Table 11. List of componentsFor test circuit see [Figure 5](#).

Component	Description	Value	Remarks
C1, C2, C6, C7, C16, C17, C23, C24	multilayer ceramic chip capacitor	1000 pF	[1]
C3	multilayer ceramic chip capacitor	47 pF	[2]
C4	multilayer ceramic chip capacitor	39 pF	[1]
C5	multilayer ceramic chip capacitor	200 pF	[1]
C8, C9, C14, C15	multilayer ceramic chip capacitor	4.7 μ F, 100 V	TDK C5750X7R2A475KT
C10, C11	electrolytic capacitor	2200 μ F, 63 V	
C12, C13	electrolytic capacitor	470 μ F, 63 V	
C18, C19	multilayer ceramic chip capacitor	120 pF	[1]
C20	multilayer ceramic chip capacitor	82 pF	[1]
C21	multilayer ceramic chip capacitor	120 pF	[1]
C22	multilayer ceramic chip capacitor	56 pF	[1]
L1, L2, L3, L4	1.5 turn 0.8 mm copper wire	D = 3.2 mm, length = 1.6 mm	
L5, L6	5.0 turn 0.8 mm copper wire	D = 3.0 mm, length = 4 mm	
L7, L8	2.5 turn 0.8 mm copper wire	D = 3.0 mm, length = 2.4 mm	
R1, R2	resistor	9.1 Ω	SMD 1206
T1	semi rigid coax	25 Ω , length = 160 mm	Micro-Coax UT-090C-25
T2	semi rigid coax	25 Ω , length = 160 mm	Micro-Coax UT-141C-25

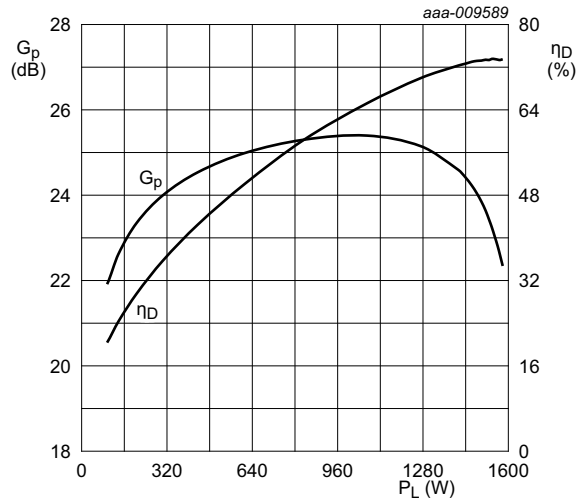
[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

7.5 Graphical data

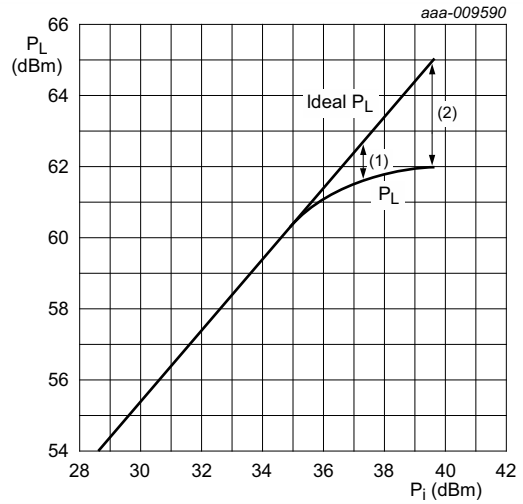
The following figures are measured in a class-AB production test circuit.

7.5.1 1-Tone CW pulsed



$V_{DS} = 50$ V; $I_{Dq} = 40$ mA; $f = 108$ MHz; $t_p = 100$ μ s; $\delta = 20$ %.

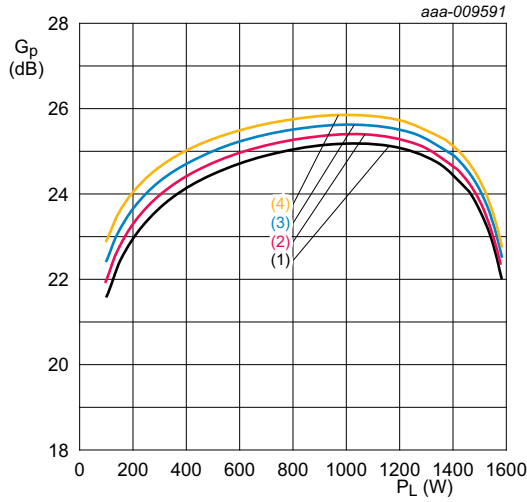
Fig 6. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 50$ V; $I_{Dq} = 40$ mA; $f = 108$ MHz; $t_p = 100$ μ s; $\delta = 20$ %.

- (1) $P_{L(1dB)} = 61.58$ dBm (1440 W)
- (2) $P_{L(3dB)} = 61.98$ dBm (1580 W)

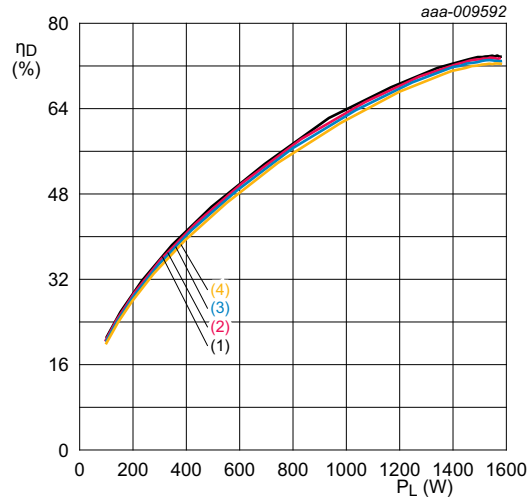
Fig 7. Output power as a function of input power; typical values



$V_{DS} = 50\text{ V}$; $f = 108\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $I_{Dq} = 20\text{ mA}$
- (2) $I_{Dq} = 40\text{ mA}$
- (3) $I_{Dq} = 80\text{ mA}$
- (4) $I_{Dq} = 160\text{ mA}$

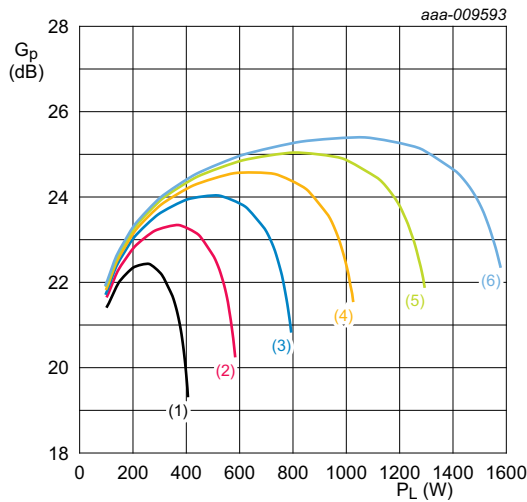
Fig 8. Power gain as a function of output power; typical values



$V_{DS} = 50\text{ V}$; $f = 108\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $I_{Dq} = 20\text{ mA}$
- (2) $I_{Dq} = 40\text{ mA}$
- (3) $I_{Dq} = 80\text{ mA}$
- (4) $I_{Dq} = 160\text{ mA}$

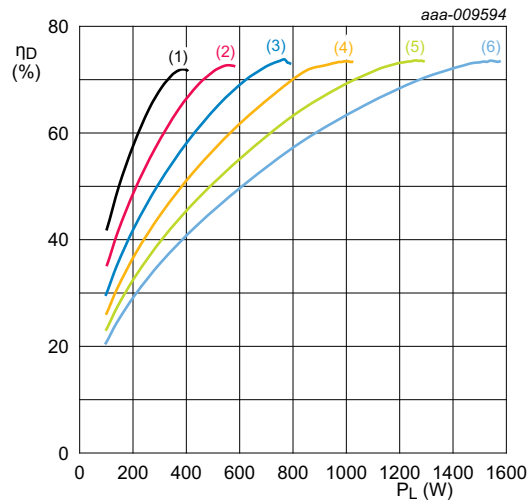
Fig 9. Drain efficiency as a function of output power; typical values



$I_{Dq} = 40\text{ mA}$; $f = 108\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $V_{DS} = 25\text{ V}$
- (2) $V_{DS} = 30\text{ V}$
- (3) $V_{DS} = 35\text{ V}$
- (4) $V_{DS} = 40\text{ V}$
- (5) $V_{DS} = 45\text{ V}$
- (6) $V_{DS} = 50\text{ V}$

Fig 10. Power gain as a function of output power; typical values



$I_{Dq} = 40\text{ mA}$; $f = 108\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $V_{DS} = 25\text{ V}$
- (2) $V_{DS} = 30\text{ V}$
- (3) $V_{DS} = 35\text{ V}$
- (4) $V_{DS} = 40\text{ V}$
- (5) $V_{DS} = 45\text{ V}$
- (6) $V_{DS} = 50\text{ V}$

Fig 11. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

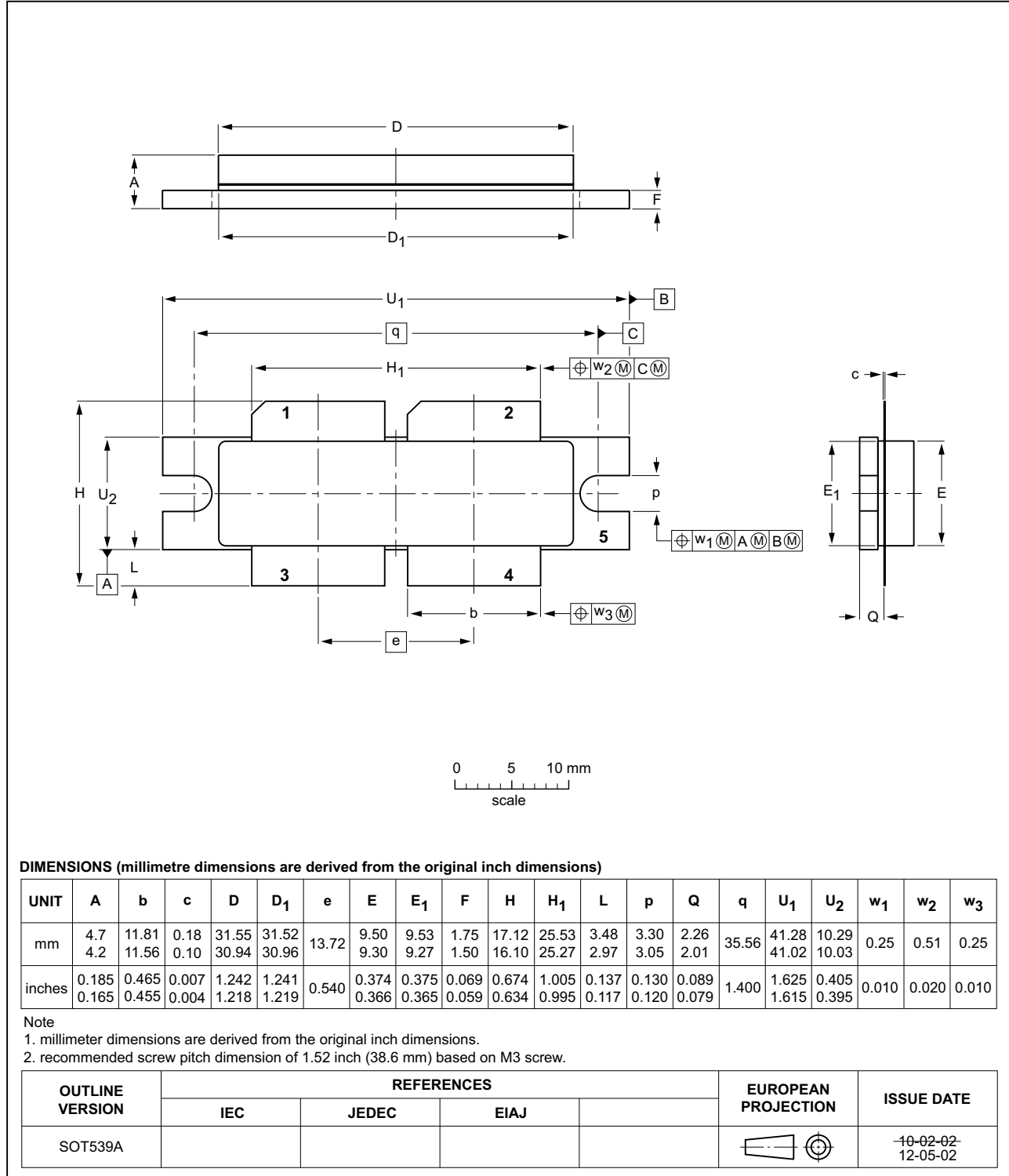


Fig 12. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

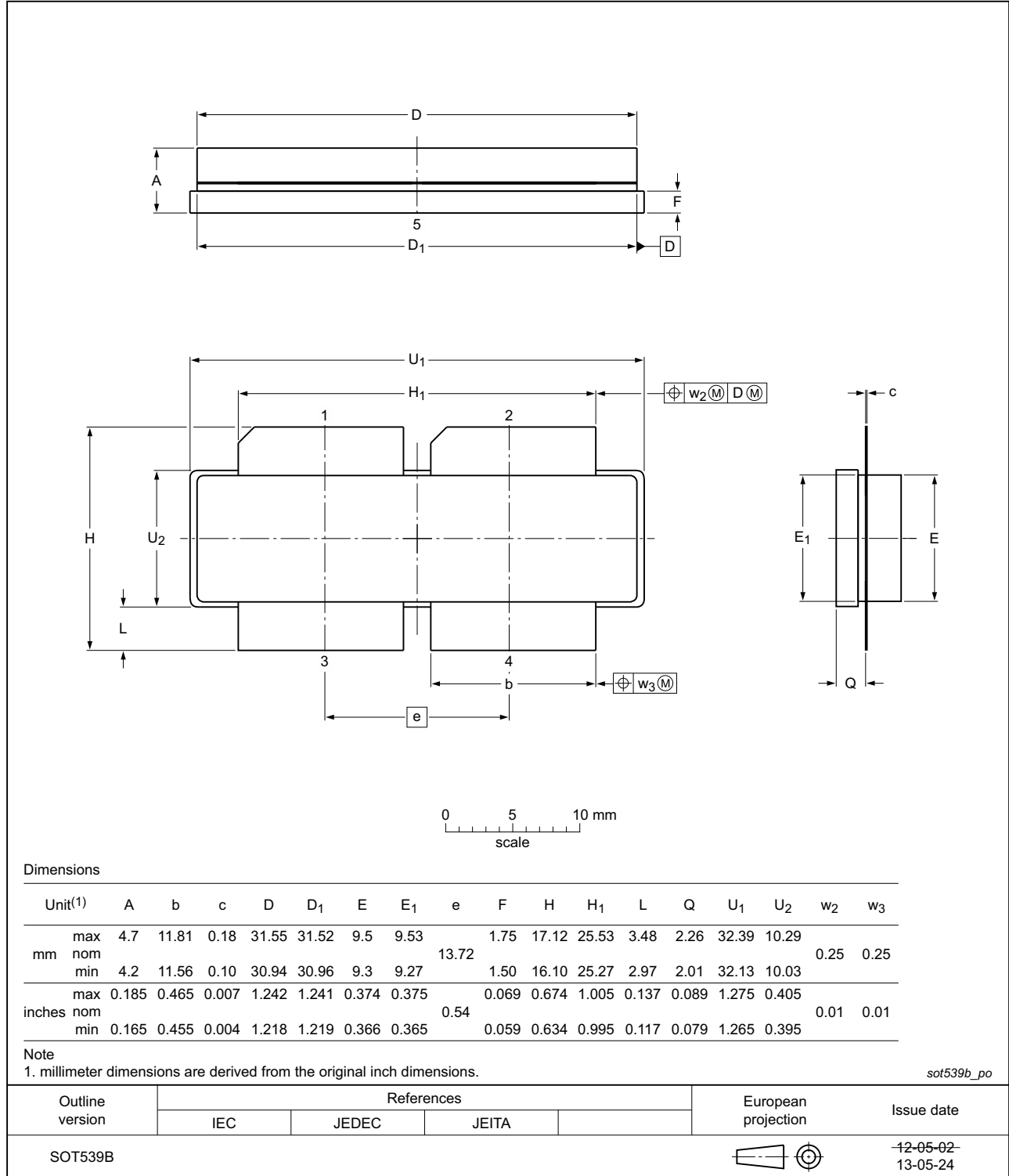


Fig 13. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
UIS	Unclamped Inductive Switching
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF188XR_BLF188XRS v.5	20131112	Product data sheet	-	BLF188XR_BLF188XRS v.4
Modifications	<ul style="list-style-type: none"> • Section 7.3 on page 5: section added 			
BLF188XR_BLF188XRS v.4	20131030	Product data sheet	-	BLF188XR_BLF188XRS v.3
BLF188XR_BLF188XRS v.3	20130801	Objective data sheet	-	BLF188XR_BLF188XRS v.2
BLF188XR_BLF188XRS v.2	20130712	Objective data sheet	-	BLF188XR_BLF188XRS v.1
BLF188XR_BLF188XRS v.1	20130506	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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